

## ASM Pacific Technology and EV Group Join Forces to Enable Industry's First Ultra Precision Die-to-Wafer Hybrid Bonding Solutions for 3D-IC Heterogeneous Integration

*Joint Development Program will offer highly configurable, ultra-precision end-to-end hybrid bonding solutions to suit various applications, with optimal line balancing and process requirements*

SINGAPORE and AUSTRIA Jan 29, 2021 – ASM PACIFIC TECHNOLOGY (ASM) and EV GROUP (EVG) announced the signing of a joint development agreement (JDA) to co-develop die-to-wafer hybrid bonding solutions for 3D-IC/heterogeneous integration applications. Die-to-wafer hybrid bonding is a pivotal process for enabling the redesign of system-on-chip (SoC) devices to 3D stacked chips via chiplet technology—combining chips with different process nodes into advanced packaging systems that can power new applications such as 5G, high-performance computing (HPC) and artificial intelligence (AI).

Heterogeneous integration is crucial to extending Moore's Law and enabling future generations of devices with increasing levels of performance. Hybrid bonding involving wafer-to-wafer as well as die-to-wafer integration is a necessary process step to support heterogeneous integration. The challenge involved in die-to-wafer hybrid bonding is to push the boundaries and confluence of technologies to achieve high throughput and high yields for mass production adoption, by blending together ultra-high-precision bonding, 'wafer fabrication' die preparation and handling in a Class 1 environment<sup>1</sup>, and hybrid and fusion bonding technologies into a fully seamless solution.

To achieve such ultra-precision, highly configurable die-to-wafer bonding capabilities requires well-matched equipment partners from the wafer fab and assembly space to come together to deliver solutions for the next level of package scaling. This is what this JDA aims to achieve. Both companies are leaders in their respective areas, with EVG's die preparation technology and front-end cleanliness for die-to-wafer hybrid bonding, and ASMPT's ultra-high precision bonding of extremely thin dies. Under the JDA, ASMPT will provide its precision die-bonding capabilities, while EVG will provide its die preparation (cleaning and activation) and wafer bonding capabilities in the form of the EVG<sup>®</sup> 320 D2W system for direct-placement die-to-wafer bonding as well as the EVG GEMINI<sup>®</sup> FB configured for collective die-to-wafer integration flows.

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<sup>1</sup> Refers to a cleanroom environment where there is no more than 1 particle of dust in a cubic foot of air.

The JDA seeks to deliver what its partners believe will be the most optimal integral customer solutions for die-to-wafer bonding to the market. The ultimate goal of die-to-wafer hybrid bonding is to reduce both the time to market and non-recurring engineering development costs by directly fusing the copper interconnects and dielectric of pre-developed chiplets of different functions to achieve improved device performance, cost and form factor. The benefits are significant, as system designers will then be able to mix and match chiplets and optimally connect them by using ASMPT's ultra-high precision (0.2µm) die placement, along with EVG's die-to-wafer hybrid bonding and fusion technologies, to achieve comparable or even better performance than SoC methodologies.

As part of the JDA, ASMPT and EVG will leverage their core competency centres in Europe and Asia to speed up the development of lead customer programs, with an eventual offering of highly-configurable modular systems to suit a full spectrum of integration and process requirements.

According to Mr. Markus Wimplinger, Corporate Technology Development and IP Director at EVG, "Heterogeneous integration provides a critical pathway forward for the semiconductor industry to realize continued innovation. EVG has invested significant resources to support this transition, by developing advanced process solutions, including industry-leading wafer-to-wafer and die-to-wafer hybrid bonding platforms, as well as creating our Heterogeneous Integration Competence Center™, which serves as an open access innovation incubator for customers and partners to accelerate the development of new and differentiating heterogeneous integration products and solutions. Underpinning all of these activities are the industry collaborations that EVG undertakes with industry leaders like ASMPT to help make these new products and solutions a reality for our customers. Through this JDA with ASMPT, which leverages our EVG320 D2W die preparation and activation system and a dedicated version of our GEMINI fusion bonding system specially configured for die-to-wafer bonding with ASMPT's benchmark die bonding solutions, we can offer the industry a complete hybrid die-to-wafer bonding process flow to help speed the deployment of heterogeneous integration technologies."

Mr. Nelson Fan, VP for Advanced Packaging, BU ICD and CIS, Semiconductor Solutions at ASMPT: "We are honoured and privileged to further extend our partnership with EVG, a pioneering leader in wet process technologies for wafer hybrid bonding. We aim to deliver the next evolution of IC interconnect solutions that will include our ultra-high precision LithoBolt™ Hybrid bonder for Chip-to-Wafer hybrid bonding and this will complement our total interconnect solutions for heterogeneous integration. We are already well positioned in

hybrid bonding with early customer engagement with lead customers such as IBM, as well as being a member of the Institute of Microelectronics' Hybrid Bonding Consortium<sup>2</sup>."

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**About ASM Pacific Technology Limited ("ASMPT")**

ASMPT (HKEX stock code: 0522) is a leading global supplier of hardware and software solutions for the manufacture of semiconductors and electronics. Headquartered in Singapore, ASMPT's offerings encompass the semiconductor assembly & packaging, and SMT (surface mount technology) industries, ranging from wafer deposition, to the various solutions that organise, assemble and package delicate electronic components into a vast range of end-user devices, which include electronics, mobile communications, computing, automotive, industrial and LED (displays). ASMPT partners with customers very closely, with continuous investment in R&D helping to provide cost-effective, industry-shaping solutions that achieve higher productivity, greater reliability and enhanced quality.

ASMPT is one of the constituent stocks of the Hang Seng TECH Index, Hang Seng Composite MidCap Index under the Hang Seng Composite Size Indexes, the Hang Seng Composite Information Technology Industry Index under Hang Seng Composite Industry Indexes and the Hang Seng Hong Kong 35 Index. To learn more about ASMPT, please visit us at [www.asmpacific.com](http://www.asmpacific.com).

**About EV Group (EVG)**

EV Group (EVG) is a leading supplier of equipment and process solutions for the manufacture of semiconductors, microelectromechanical systems (MEMS), compound semiconductors, power devices and nanotechnology devices. Key products include wafer bonding, thin-wafer processing, lithography/nanoimprint lithography (NIL) and metrology equipment, as well as photoresist coaters, cleaners and inspection systems. Founded in 1980, EV Group services and supports an elaborate network of global customers and partners all over the world. More information about EVG is available at [www.EVGroup.com](http://www.EVGroup.com).

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<sup>2</sup> The Institute of Microelectronics (IME) is a research institute of the Singapore Agency for Science, Technology and Research (A\*STAR). Its missions is to strategically add value to Singapore's semiconductor industry. Key research areas are in Heterogeneous Integration, System-in-Package, Sensor, Actuators and Microsystems, RF & mmWave, SiC/GaN-on-SiC Power Electronics, and MedTech.